

Title (en)
Memory circuit having compressed testing function

Title (de)
Speicherschaltung mit komprimierter Testfunktion

Title (fr)
Circuit mémoire avec fonction de test comprimé

Publication
EP 1316966 A3 20060322 (EN)

Application
EP 02257282 A 20021021

Priority
JP 2001363871 A 20011129

Abstract (en)
[origin: EP1316966A2] A multi-bit output configuration memory circuit comprises: a memory core (10) having a normal cell array and a redundant cell array, which have a plurality of memory cells; N output terminals (DQ1-DQ4) which collectively output N-bit data read out from the memory core (10); and an output circuit (2) provided between the output terminals and the memory core, which divides the N-bit data into M groups each of L bits ($N = L \times M$), and detects whether the L bits of each group match or not. The output circuit (2) outputs a compressed output which becomes the output data in the event of a match and which becomes a third state in the event of a non-match, to a first output terminal (DQ1) of the N output terminals (DQ1-DQ4). Responding to each of a plurality of test commands or test control signals applied to external terminals, the compressed output of the M groups of L-bit output is outputted in a time-division manner.

IPC 8 full level
G01R 31/28 (2006.01); **G01R 31/3185** (2006.01); **G11C 29/00** (2006.01); **G11C 29/14** (2006.01); **G11C 29/34** (2006.01); **G11C 29/38** (2006.01); **G11C 29/40** (2006.01)

CPC (source: EP KR US)
G11C 29/00 (2013.01 - KR); **G11C 29/40** (2013.01 - EP US)

Citation (search report)

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- [A] US 6252805 B1 20010626 - SO BYUNG-SE [KR], et al
- [A] US 5652725 A 19970729 - SUMA KATSUHIRO [JP], et al & US 6643805 B1 20031104 - KIKUTAKE AKIRA [JP], et al
- [A] PATENT ABSTRACTS OF JAPAN vol. 2000, no. 15 6 April 2001 (2001-04-06)

Designated contracting state (EPC)
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR

DOCDB simple family (publication)
EP 1316966 A2 20030604; **EP 1316966 A3 20060322**; **EP 1316966 B1 20080910**; CN 1252730 C 20060419; CN 1421868 A 20030604; DE 60228809 D1 20081023; JP 2003168299 A 20030613; JP 3874653 B2 20070131; KR 100822980 B1 20080416; KR 20030044782 A 20030609; TW 594777 B 20040621; US 2003099143 A1 20030529; US 6731553 B2 20040504

DOCDB simple family (application)
EP 02257282 A 20021021; CN 02154365 A 20021129; DE 60228809 T 20021021; JP 2001363871 A 20011129; KR 20020065765 A 20021028; TW 91123963 A 20021017; US 27019602 A 20021015