

Title (en)  
Memory circuit having compressed testing function

Title (de)  
Speicherschaltung mit komprimierter Testfunktion

Title (fr)  
Circuit mémoire avec fonction de test comprimé

Publication  
**EP 1316966 A3 20060322 (EN)**

Application  
**EP 02257282 A 20021021**

Priority  
JP 2001363871 A 20011129

Abstract (en)  
[origin: EP1316966A2] A multi-bit output configuration memory circuit comprises: a memory core (10) having a normal cell array and a redundant cell array, which have a plurality of memory cells; N output terminals (DQ1-DQ4) which collectively output N-bit data read out from the memory core (10); and an output circuit (2) provided between the output terminals and the memory core, which divides the N-bit data into M groups each of L bits ( $N = L \times M$ ), and detects whether the L bits of each group match or not. The output circuit (2) outputs a compressed output which becomes the output data in the event of a match and which becomes a third state in the event of a non-match, to a first output terminal (DQ1) of the N output terminals (DQ1-DQ4). Responding to each of a plurality of test commands or test control signals applied to external terminals, the compressed output of the M groups of L-bit output is outputted in a time-division manner.

IPC 8 full level  
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Citation (search report)

- [A] US 6324087 B1 20011127 - PEREIRA JOSE PIO [US]
- [A] US 6252805 B1 20010626 - SO BYUNG-SE [KR], et al
- [A] US 5652725 A 19970729 - SUMA KATSUHIRO [JP], et al & US 6643805 B1 20031104 - KIKUTAKE AKIRA [JP], et al
- [A] PATENT ABSTRACTS OF JAPAN vol. 2000, no. 15 6 April 2001 (2001-04-06)

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