

Title (en)

SILICON OXIDE PATTERNING USING CVD PHOTORESIST

Title (de)

SILIZIUMOXYDSTRUKTURIERUNG MITTELS CVD-PHOTOLACKS

Title (fr)

MODELAGE D'OXYDE DE SILICIUM AU MOYEN D'UN PHOTORESIST CVD

Publication

**EP 1320877 A2 20030625 (EN)**

Application

**EP 01964510 A 20010830**

Priority

- US 0126999 W 20010830
- US 67074300 A 20000927

Abstract (en)

[origin: WO022777A2] An integrated circuit, and method of forming thereof, comprising CVD photoresist (e.g., PPMS 202) is formed on a substrate (e.g., silicon 200), patterned and converted into silicon oxide, and is left on the substrate to function as a silicon oxide layer (e.g., PPMSO 204). A high quality cap layer (e.g., PECVD silicon oxide 212) may then be formed over the lower quality silicon oxide layer utilizing a maskless etch process. A high quality silicon oxide layer (e.g. silicon oxide 308) may be formed on the substrate prior to formation of the CVD photoresist layer to provide a buffer underneath the lower quality silicon oxide. Because etch selectivity is generally not required for the photoresist layer, a thinner photoresist may be used than that of prior art techniques, permitting a larger lithographic process window, increased depth of focus, and a more robust process.

IPC 1-7

**H01L 21/312**

IPC 8 full level

**H01L 21/312** (2006.01)

CPC (source: EP KR)

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Citation (search report)

See references of WO 022777A2

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