Title (en)

Semiconductor input/output circuit arrangement

Title (de)

Eingangs/Ausgangs-Schaltungsanordnung für einen integrierten Halbleiterbaustein

Title (fr)

Système de circuit d'entrée/sortie dans un circuit intégré à semi-conducteur

Publication

EP 1321984 A2 20030625 (EN)

Application

EP 01307231 A 20010824

Priority

EP 01307231 A 20010824

Abstract (en)

A method of producing a semiconductor circuit is disclosed with an area saving in comparison to conventional circuit layouts. IO cells are arranged with a width multiplied by a factor, but with corresponding reduced height. ESD protection circuitry is included at a reduced rate in comparison to usual arrangements. The space saving is achieved by occupying a semiconductor area that would have been used by ESD circuitry with the IO circuitry. ESD protection is maintained but at different locations. <IMAGE>

IPC 1-7

H01L 27/118; H01L 27/02; H01L 23/528

IPC 8 full level

H01L 23/528 (2006.01); **H01L 27/02** (2006.01)

CPC (source: EP US)

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Designated contracting state (EPC)

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DOCDB simple family (publication)

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DOCDB simple family (application)

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