

Title (en)
PLANAR DIAC

Title (de)
PLANAR-DIAC

Title (fr)
DIAC PLANAR

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Application
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Abstract (en)
[origin: FR2815472A1] The diac comprises a substrate (21) of highly doped n-type conductivity, an epitaxial layer (22) of lightly doped p-type conductivity on the side of the upper surface of the epitaxial layer, a channel-restraining ring (25) of p-type conductivity with higher doping level than that of the epitaxial layer and formed at the exterior of the region (24), a peripheral wall (26) of highly doped n-type conductivity at the exterior of the ring (25), extending vertically and joining the substrate, and metallic layers (M1,M2). The channel-restraining ring (25) has the role of suppressing leakage currents flowing in a region below the upper surface of the epitaxial layer (22) from the metallic layer (M1) towards the metallic layer (M2) by the intermediary of peripheral wall (26) and the substrate (21). The region (24) extends to about 5 micrometer from the upper surface of the epitaxial layer, and the set including the region (23) and the layer (22) extends to about 12 micrometer. The diac is asymmetrical, and the breakdown voltages are 32 V and -50 V. A symmetrical diac can be formed by assembling two asymmetrical diacs in antiparallel configuration. The antiparallel assembly comprises the first diac soldered by the rear surface on a conducting plate, the second diac soldered by the rear surface on another conducting plate, and the front surface of each diac soldered by a wire to the conducting plate carrying the other diac.

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