

Title (en)

POLY FUSE ROM WITH MOS DEVICE BASED CELL STRUCTURE AND THE METHOD FOR READ AND WRITE THEREFORE

Title (de)

ROM AUS MEHREREN SICHERUNGEN MIT AUF MOS ANORDNUNG BASIERENDER ZELLSTRUKTUR UND LESE- UND SCHREIBVERFAHREN DAFÜR

Title (fr)

MEMOIRE ROM A FUSIBLES MULTIPLES COMPRENANT UNE STRUCTURE DE CELLULES A DISPOSITIF MOS ET PROCEDE DE LECTURE ET D'ECRITURE POUR CETTE MEMOIRE

Publication

**EP 1340262 A2 20030903 (EN)**

Application

**EP 01997848 A 20011119**

Priority

- EP 0113467 W 20011119
- US 72341300 A 20001127

Abstract (en)

[origin: WO0243152A2] A one-time programmable (OTP) structure is implemented using a self-aligned silicided (SALICIDE) poly-silicon fuse. In an example embodiment, the OTP structure is laid out as a fuse element having a first terminal and a second terminal. A switching transistor having a drain, source, and a gate surrounds the fuse element. The drain is coupled to the second terminal of the fuse element surrounds the fuse element. The gate surrounds the drain. The source surrounds the gate. To build transistor with sufficient drive capability for programming the fuse element, the geometry of the gate is laid out in a serpentine or an equivalent pattern increase the effective W/L. A feature of this layout is that OTP cells may be abutted to one-another to form an array. Metallization is arranged so that row lines connect to the first terminal of the fuse element and column lines connect to the gate of the switching transistor. The arrangement enables the placing of read and write circuits at opposite sides of the array. All of the gates in a column may be read simultaneously while providing write current to program one fuse at a time.

IPC 1-7

**H01L 27/112**; **H01L 21/8246**

IPC 8 full level

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CPC (source: EP)

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C-Set (source: EP)

**H01L 2924/0002** + **H01L 2924/00**

Citation (examination)

- US 5742087 A 19980421 - LIDOW ALEXANDER [US], et al
- US 5854510 A 19981229 - SUR JR HARLAN LEE [US], et al
- See also references of WO 0243152A2

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