Title (en)

PARALLEL ELECTRONIC ARCHITECTURE COMPRISING A PLURALITY OF PROCESSING UNITS CONNECTED TO A COMMUNICATION BUS, AND ADDRESSABLE BY THEIR FUNCTIONAL CAPABILITIES

Title (de)

PARALLELE ELEKTRONISCHE ARCHITEKTUR MIT MEHREREN AN EINEM KOMMUNIKATIONSBUS ANGESCHLOSSENEN UND FUNKTIONALITÄTSADRESSIERBAREN VERARBEITUNGSEINHEITEN

Title (fr)

ARCHITECTURE ELECTRONIQUE PARALLELE COMPORTANT UNE PLURALITE D'UNITES DE TRAITEMENT CONNECTEES A UN BUS DE COMMUNICATION, ET ADRESSABLES PAR LEURS FONCTIONNALITES

Publication

EP 1344131 A1 20030917 (FR)

Application

EP 01995776 A 20011221

Priority

• FR 0104176 W 20011221
• FR 0016858 A 20001222

Abstract (en)

[origin: WO02052414A1] The invention concerns a parallel electronic architecture comprising a plurality of processing units (1a, 1b, , 1n) connected to a communication bus, each processing unit being designed to automatically execute one or several predefined tasks. Each processing unit is configured such that each of the tasks is associated with a function key, and designed to communicate with the other processing units in accordance with the following protocol: transmission of a message comprising at least a function key characterising a functional capability, and optionally a frame consisting of one or several words; each processing unit is further designed to decode each header passing through the bus, and, on the basis of the value of said function key, to either ignore the message transmitted on the bus, or execute the task associated with said message function key.

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G06F 9/48

IPC 8 full level

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