

Title (en)
MRAM ARCHITECTURE AND SYSTEM

Title (de)
MRAM ARCHITEKTUR UND SYSTEM

Title (fr)
ARCHITECTURE ET SYSTEME DE MRAM

Publication
EP 1358655 A2 20031105 (EN)

Application
EP 02709023 A 20020111

Priority
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Abstract (en)
[origin: US6418046B1] A magnetoresistive memory fabricated on a common substrate. The memory including first and second spaced apart magnetoresistive memory arrays each including a plurality of MTJ memory cells arranged in rows and columns and a plurality of word/digit lines associated with the rows of magnetoresistive memory cells of each of the arrays. Switching circuitry is positioned on the substrate between the first and second arrays and designed to select a word/digit line in one of the first and second arrays. A current source is positioned on the substrate adjacent and coupled to the switching circuitry for supplying programming current to the selected word/digit line.

IPC 1-7
G11C 5/00

IPC 8 full level
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CPC (source: EP KR US)
G11C 11/15 (2013.01 - KR); **G11C 11/16** (2013.01 - EP US); **G11C 11/1657** (2013.01 - EP US)

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US 2002101760 A1 20020801; **US 6418046 B1 20020709**; AU 2002243531 A1 20020812; CN 100390898 C 20080528; CN 1496569 A 20040512; DE 60229216 D1 20081120; EP 1358655 A2 20031105; EP 1358655 B1 20081008; JP 2004530240 A 20040930; JP 2008257866 A 20081023; JP 4834040 B2 20111207; KR 100869658 B1 20081121; KR 20030072616 A 20030915; TW 546652 B 20030811; US 2002131295 A1 20020919; US 6552927 B2 20030422; WO 02061752 A2 20020808; WO 02061752 A3 20021024

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