

Title (en)

Architecture for controlling dissipated power in a system on a chip and related system

Title (de)

Einchip-Systemarchitektur zur Verlustleistungskontrolle und verwandtes System

Title (fr)

Architecture d'un système sur une puce pour le contrôle de la puissance dissipée et système associé

Publication

**EP 1363179 A1 20031119 (EN)**

Application

**EP 02011094 A 20020517**

Priority

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Abstract (en)

A system-on-chip (SoC) architecture includes a plurality of blocks (12; M1, M2, ..., Mn; S1, S2, ..., Sk), each including a power control module (20) to selectively control the power dissipated by the block: For each block of said plurality (12; M1, M2, ..., Mn; S1, S2, ..., Sk) a power register (PCR) is provided to receive power control instructions to selectively control the respective power control module (20). The system also includes a power control unit (16) for writing respective power control instructions into the power control registers (PCR) of the blocks, whereby the power dissipated is controlled individually and independently for each block under the centralized control of the power control unit (16). For each block (12; M1, M2, ..., Mn; S1, S2, ..., Sk), a power status register (PSR) is also provided to receive status information concerning power control within the respective block. The power control unit (16) is arranged to read said status instructions from such the power status registers (PSR). <IMAGE>

IPC 1-7

**G06F 1/32**; **H01L 23/34**

IPC 8 full level

**G06F 1/32** (2006.01); **H01L 23/34** (2006.01)

CPC (source: EP US)

**G06F 1/3203** (2013.01 - EP US); **G06F 1/3237** (2013.01 - EP US); **G06F 1/324** (2013.01 - EP US); **G06F 1/3243** (2013.01 - EP US); **G06F 1/3287** (2013.01 - EP US); **G06F 9/30101** (2013.01 - EP US); **H01L 23/34** (2013.01 - EP US); **H01L 2924/0002** (2013.01 - EP US); **Y02D 10/00** (2017.12 - EP US)

Citation (search report)

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Designated contracting state (EPC)

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DOCDB simple family (application)

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