

Title (en)
Multilayer printed circuit board laminate and process for manufacturing the same

Title (de)
Mehrlagen-Leiterplatten-Verbundkörper sowie Verfahren zu dessen Herstellung

Title (fr)
Laminé de panneau à circuit imprimé multicouche et son procédé de fabrication

Publication
EP 1363483 A3 20051005 (DE)

Application
EP 03010758 A 20030514

Priority
DE 10221553 A 20020514

Abstract (en)
[origin: EP1363483A2] The method involves providing a circuit board blank (1) comprising a substrate (2) and at least one electrically conductive layer (3) of a thickness that is suitable for carrying power currents. The thickness of part of the conductive layer (3) is reduced to create a signal conduction layer. The conductive layer has a thickness DL, where 150 mumat mostDLapproximately600 mum, preferably DL400 mum. An Independent claim is included for a multilayer circuit board module.

IPC 1-7
H05K 3/06; **H05K 1/02**

IPC 8 full level
H05K 1/02 (2006.01); **H05K 3/06** (2006.01); **H05K 1/00** (2006.01); **H05K 3/42** (2006.01)

CPC (source: EP)
H05K 1/0265 (2013.01); **H05K 3/06** (2013.01); **H05K 1/0393** (2013.01); **H05K 3/427** (2013.01); **H05K 2201/0394** (2013.01); **H05K 2201/09736** (2013.01); **H05K 2203/1476** (2013.01); **H05K 2203/302** (2013.01)

Citation (search report)
• [AY] EP 0843507 A2 19980520 - MECANISMOS AUX IND [ES]
• [AY] US 6222136 B1 20010424 - APPELT BERND KARL-HEINZ [US], et al
• [Y] DE 4208765 A1 19930805 - MECANISMOS AUX IND [ES]
• [XY] PATENT ABSTRACTS OF JAPAN vol. 018, no. 673 (E - 1647) 19 December 1994 (1994-12-19)
• [XA] PATENT ABSTRACTS OF JAPAN vol. 014, no. 032 (E - 876) 22 January 1990 (1990-01-22)
• [XA] DATABASE WPI Week 198738, Derwent World Patents Index; AN 1987-267256, XP002340294
• [A] PATENT ABSTRACTS OF JAPAN vol. 018, no. 590 (E - 1628) 10 November 1994 (1994-11-10)
• [A] PATENT ABSTRACTS OF JAPAN vol. 2000, no. 25 12 April 2001 (2001-04-12)

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Designated contracting state (EPC)
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR

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