

Title (en)
HARVARD ARCHITECTURE MICROPROCESSOR HAVING A LINEAR ADDRESSABLE SPACE

Title (de)
HARVARD-ARCHITEKTUR-MIKROPROZESSOR MIT EINEM ADRESSIEBAREN LINEAREN BEREICH

Title (fr)
MICROPROCESSEUR A ARCHITECTURE HARVARD AYANT UN ESPACE ADRESSABLE LINEAIRE

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Application
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• FR 0102701 A 20010228

Abstract (en)
[origin: FR2821456A1] The invention relates to a microprocessor which is connected to a first memory space (4) by means of a first bus (AP, DIP, DOP, RWP) and to a second memory space (5) by means of a second bus (AD, DID, DODD, RWD). The inventive microprocessor comprises a processing unit (2), which is fitted with a program bus (PC, INS) and a data bus (A, DBO, DBI, RW), and an interface unit (3) which is connected, on one side, to the program bus (PC, INS) and the data bus (A, DBO, DBI, RW) and, on the other side, to the first bus (AP, DIP, DOP, RWP) and the second bus (AD, DID, DOP, RWD). The interface unit (3) comprises switching means (23, 25, 26) for connecting the program bus and the data bus respectively either to the first bus or the second bus according to the requests sent by the processing unit for access to the program (NPR) and to the data (NDR) respectively.

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