Title (en)

CIRCUIT AND METHOD FOR TEST AND REPAIR

Title (de)

SCHALTUNG UND VERFAHREN ZUR PRÜFUNG UND REPARATUR

Title (fr)

CIRCUIT ET PROCEDE DE TEST ET DE REPARATION

Publication

EP 1368812 A2 20031210 (EN)

Application

EP 02766724 A 20020311

Priority

- US 0207270 W 20020311
- US 81036601 A 20010315

Abstract (en)

[origin: US6918072B2] Circuitry is provided to allow early switching of input signals from a first configuration directed to blow a first anti-fuse to a second configuration directed to blow a second anti-fuse, yet still allow complete blowing of the first anti-fuse. Such circuitry may be applied to methods of repairing a memory device after testing. Data concerning available repair cells may be stored in at least one on-chip redundancy register.

IPC 1-7

G11C 29/00

IPC 8 full level

G01R 31/28 (2006.01); **G11C 11/401** (2006.01); **G11C 11/413** (2006.01); **G11C 16/02** (2006.01); **G11C 29/00** (2006.01); **G11C 29/12** (2006.01); **G11C 29/44** (2006.01)

CPC (source: EP KR US)

G11C 29/00 (2013.01 - KR); **G11C 29/44** (2013.01 - EP US); **G11C 29/72** (2013.01 - EP US)

Designated contracting state (EPC)

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

DOCDB simple family (publication)

US 2002133767 A1 20020919; **US 6904552 B2 20050607**; AT E430980 T1 20090515; AU 2002338564 A1 20021111; CN 100483557 C 20090429; CN 1509479 A 20040630; DE 60232227 D1 20090618; EP 1368812 A2 20031210; EP 1368812 B1 20090506; JP 2004528669 A 20040916; JP 4027805 B2 20071226; KR 100559022 B1 20060310; KR 20040041540 A 20040517; US 2002133770 A1 20020919; US 6918072 B2 20050712; WO 02089147 A2 20021107; WO 02089147 A3 20030501

DOCDB simple family (application)

US 81036601 A 20010315; AT 02766724 T 20020311; AU 2002338564 A 20020311; CN 02809883 A 20020311; DE 60232227 T 20020311; EP 02766724 A 20020311; JP 2002586357 A 20020311; KR 20037011999 A 20030915; US 0207270 W 20020311; US 86468201 A 20010524