Title (en)

Integrated circuit device with clock skew reduced

Title (de)

Integrierte Schaltunganordnung mit reduzierter Taktverschiebung

Title (fr)

Circuit intégré à décalage réduit

Publication

EP 1383025 A3 20041110 (EN)

Application

EP 03012270 A 20030611

Priority

JP 2002170836 A 20020612

Abstract (en)

[origin: US2003231043A1] In an integrated circuit device, a clock signal distribution section is arranged in an outer circumferential area of a semiconductor chip to supply a clock signal. Each of interface circuit blocks has at least an internal circuit operating based on the clock signal supplied from the clock signal distribution section.

IPC 1-7

G06F 1/10

IPC 8 full level

G06F 1/10 (2006.01); **H01L 21/82** (2006.01); **H01L 21/822** (2006.01); **H01L 27/04** (2006.01); **H03K 5/15** (2006.01)

CPC (source: EP US)

G06F 1/10 (2013.01 - EP US)

Citation (search report)

- [X] US 5696953 A 19971209 - WONG KENG L [US], et al
- [X] US 5396129 A 19950307 - TABIRA YOSHIHIRO [JP]
- [X] EP 0258975 A2 19880309 - ETA SYSTEMS INC [US]
- [X] US 5172330 A 19921215 - WATANABE HIROYUKI [JP], et al
- [A] US 6201448 B1 20010313 - TAM SIMON M [US], et al

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR

DOCDB simple family (publication)

US 2003231043 A1 20031218; **US 7005907 B2 20060228**; AU 2003204630 A1 20040115; EP 1383025 A2 20040121; EP 1383025 A3 20041110; JP 2004015032 A 20040115; JP 3767520 B2 20060419

DOCDB simple family (application)

US 45864303 A 20030611; AU 2003204630 A 20030611; EP 03012270 A 20030611; JP 2002170836 A 20020612