

Title (en)

DRAM CELL ARRANGEMENT WITH VERTICAL MOS TRANSISTORS AND METHOD FOR THE PRODUCTION THEREOF

Title (de)

DRAM-ZELLENANORDNUNG MIT VERTIKALEN MOS-TRANSISTOREN UND VERFAHREN ZU DEREN HERSTELLUNG

Title (fr)

DISPOSITIF DE CELLULES DRAM COMPORTANT DES TRANSISTORS MOS VERTICAUX ET PROCEDE DE FABRICATION

Publication

EP 1396026 A2 20040310 (DE)

Application

EP 02740639 A 20020523

Priority

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Abstract (en)

[origin: DE10125967C1] The channel regions, which are arranged along one of the columns of the storage cell matrix, are parts of a connecting element surrounded by a gate dielectric layer. The gate electrodes of the MOS transistors of a row are parts of a strip-shaped word line. According to the invention, a vertical double gate MOS transistor having gate electrodes, which are formed in the trenches on both sides of the assigned connecting element, of the assigned word line, is provided at each point of intersection of the storage cell matrix.

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IPC 8 full level

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