

Title (en)

MEMORY CELL, MEMORY CELL CONFIGURATION AND METHOD FOR PRODUCING THE SAME

Title (de)

SPEICHERZELLE, SPEICHERZELLENANORDNUNG UND HERSTELLUNGSVERFAHREN

Title (fr)

CELLULE DE MEMOIRE, DISPOSITIF A CELLULES DE MEMOIRE, ET PROCEDE DE FABRICATION Y RELATIF

Publication

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Application

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Abstract (en)

[origin: WO03001600A2] The invention relates to memory transistors with trenched gate electrodes (2) and an ONO memory layer sequence (5, 6, 7), whose source/drain regions (3, 4) are associated with an electroconductive layer (8) or layer sequence that has a strip-shaped structure that corresponds to the bit lines. Said layer especially comprises a metal silicide or a polysilicon layer (14) with a metallic layer (15) applied thereto that reduces the ohmic resistance of the trenched bit lines. The metal silicide is preferably a cobalt silicide, the metallic layer is preferably a tungsten silicide or WN/W.

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IPC 8 full level

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