

Title (en)  
NON-POWER-OF-TWO GRAY-CODE COUNTER SYSTEM HAVING BINARY INCREMENTER WITH COUNTS DISTRIBUTED WITH BILATERAL SYMMETRY

Title (de)  
NICHT AUF ZWEIERPOTENZ BASIERENDES GRAY-CODE ZÄHLERSYSTEM MIT EINEM BINÄREN INCREMENTIERER MIT ZWEISEITIG SYMMETRISCH VERTEILTEN ZAHLEN

Title (fr)  
COMPTEUR EN CODE GRAY NON PROGRAMMABLE EN PUISSANCE DE DEUX POURVU D'UN INCREMENTEUR BINAIRE DONT LES COMPTAGES SONT REPARTIS SELON UNE SYMETRIE BILATERALE

Publication  
**EP 1410509 A2 20040421 (EN)**

Application  
**EP 01978284 A 20010817**

Priority  
• EP 0109573 W 20010817  
• US 64434800 A 20000823

Abstract (en)  
[origin: US6337893B1] A gray-code counter system (AP1) for a RAM-based FIFO comprises a read pointer (10), a write pointer (20), and a detector (30). The read pointer includes a gray-code decoder (11), a binary incrementer (12), a gray-code encoder (13), and a register (14) that holds the pointer count). The binary incrementer increments by 1 except when the input is 0110 (decimal 6) or 1110 (decimal 14); in these cases, it increments by 3. The result is a 4-bit modulo-12 gray-code sequence with the twelve allowed gray-code values being distributed among the sixteen possible 4-bit gray code values with translational and reflective bilateral symmetry. The write pointer is similar. Because of the translational symmetry, detectors that work with counters with modulo numbers that are power of two work with the corresponding non-power-of-two counter to provide "full" and "empty" indications. When read and write counts differ at the two most-significant bit positions but are equal at the remaining bit positions, the detector provides a "full" indication for a 6-count FIFO. The gray-code counter design is scaleable to any non-power-of-two modulo number divisible by four.

IPC 1-7  
**H03K 23/00**

IPC 8 full level  
**G06F 5/12** (2006.01); **G06F 5/10** (2006.01); **G06F 5/14** (2006.01); **H03K 23/00** (2006.01); **H03K 23/66** (2006.01); **H03M 7/16** (2006.01)

CPC (source: EP US)  
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