Title (en)

EFFICIENT INTERRUPT SYSTEM FOR SYSTEM ON CHIP DESIGN

Title (de)

EFFIZIENTES UNTERBRECHUNGSSYSTEM FÜR ON-CHIP SYSTEMENENTWURF

Title (fr)

SYSTEME D'INTERRUPTION EFFICACE POUR SYSTEME SUR PUCE

Publication

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Application

EP 02745724 A 20020702

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Abstract (en)

[origin: WO03012658A1] A method (400) and system (10) for managing interrupts in a system on a chip design that includes multiple processors (100a, 100b, ..., 100n) coupled to multiple peripheral devices (120a, 120b, ..., 120m). A plurality of interconnected interrupt controllers (110a, 110b, ..., 110n) are coupled between the processors and the peripheral devices. Interrupts generated by the peripheral devices are received by all of the interrupt controllers. In one embodiment, an interrupt controller is paired with a processor. Each interrupt controller can identify which interrupts will be passed to its respective processor. The interrupt controllers work in concert to pass each interrupt to a particular processor.

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G06F 13/26

IPC 8 full level

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