

Title (en)
INTERRUPT-CONTROLLER

Title (de)
UNTERBRECHER-STEUEREINRICHTUNG

Title (fr)
DISPOSITIF DE COMMANDE D'INTERRUPTION

Publication
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Application
EP 01990568 A 20011214

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Abstract (en)
[origin: WO0248880A2] The invention relates to an interrupt controller for controlling the accessing of a processor (100) by interrupt sources (11, 12, 13, 14) and for controlling the associated branching of the signal processing programme (Rx) that is being executed with a current priority (Px) in the processor. The input side of the interrupt controller contains a predetermined number of interrupt interfaces (21, 22, 23, 24) for connecting the interrupt sources and a priority value (Pi) and an address (Adi) is allocated to each interrupt interface (21, 22, 23, 24). A selection device (30) determines the interrupt interfaces that have the highest priority value (Pmax) amongst the activated interrupt interfaces. The multiplexing of the individual interrupt interfaces (21, 22, 23, 24) to the processor (100) as an interrupt request (IR) is dependent on a priority comparator (40) and a branching logic (60), which control the triggering of a context backup (I) in the processor (100), based on the determined priority value (Pmax) and the current priority value (Px). If possible, the branching logic only determines the associated branching addresses (Vi) at the end of the context backup (I) that is being executed, in order to take into consideration the interrupt requests that are received during said context backup (I).

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