

Title (en)

FORMING A SEMICONDUCTOR STRUCTURE USING A COMBINATION OF PLANARIZING METHODS AND ELECTROPOLISHING

Title (de)

BILDUNG EINER HALBLEITERSTRUKTUR UNTER VERWENDUNG EINER KOMBINATION VON PLANARISIERUNGSVERFAHREN UND ELEKTROPOLOPIEREN

Title (fr)

FORMATION D'UNE STRUCTURE A SEMI-CONDUCTEUR AU MOYEN D'UNE COMBINAISON DE PROCEDE DE PLANARISATION ET DE POLISSAGE ELECTROLYTIQUE

Publication

EP 1423868 A2 20040602 (EN)

Application

EP 02773205 A 20020815

Priority

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- US 31308601 P 20010817

Abstract (en)

[origin: WO03017330A2] A method for planarizing and electropolishing a conductive layer on a semiconductor structure includes forming a dielectric layer with recessed areas and non-recessed areas on the semiconductor wafer. A conductive layer is formed over the dielectric layer to cover the recessed areas and non-recessed areas. The surface of the conductive layer is then planarized to reduce variations in the topology of the surface. The planarized conductive layer is then electropolished to expose the non-recessed area.

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H01L 21/302

IPC 8 full level

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CPC (source: EP KR)

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