

Title (en)

MULTI-RATE SHARED MEMORY ARCHITECTURE FOR FRAME STORAGE AND SWITCHING

Title (de)

MEHRRATEN-SHARED-MEMORY-ARCHITEKTUR FÜR DIE RAHMENSPEICHERUNG UND VERMITTLUNG

Title (fr)

ARCHITECTURE DE MEMOIRE PARTAGEE A PLUSIEURS CADENCES POUR MEMORISATION ET COMMUTATION DE TRAMES

Publication

**EP 1425672 B1 20080206 (EN)**

Application

**EP 02709739 A 20020227**

Priority

- US 0206228 W 20020227
- US 93222301 A 20010817

Abstract (en)

[origin: WO03017115A1] A shared memory (120) provides buffering and switching for all data frames that flow through a network channel switch. Received frames of data are written to shared memory via the receiving (RX) port and read from shared memory by the transmitting (TX) port. Shared memory allows data to be written to a buffer at one rate and read from a buffer at a different rate.

IPC 8 full level

**G06F 13/14** (2006.01); **G06F 13/00** (2006.01); **G06F 13/16** (2006.01); **G06F 13/36** (2006.01); **G06F 13/40** (2006.01); **H04L 12/56** (2006.01)

CPC (source: EP US)

**G06F 13/1689** (2013.01 - EP US); **G06F 13/4022** (2013.01 - EP US); **H04L 49/357** (2013.01 - EP US); **H04L 49/103** (2013.01 - EP US); **H04L 49/254** (2013.01 - EP US)

Designated contracting state (EPC)

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

DOCDB simple family (publication)

**WO 03017115 A1 20030227**; AT E385591 T1 20080215; DE 60224939 D1 20080320; DE 60224939 T2 20090205; EP 1425672 A1 20040609; EP 1425672 A4 20060719; EP 1425672 B1 20080206; US 2003046496 A1 20030306; US 2007002861 A1 20070104; US 7054312 B2 20060530

DOCDB simple family (application)

**US 0206228 W 20020227**; AT 02709739 T 20020227; DE 60224939 T 20020227; EP 02709739 A 20020227; US 44463206 A 20060530; US 93222301 A 20010817