

Title (en)

Methods and apparatus for verifying the operation of a circuit design

Title (de)

Verfahren und Gerät zur Prüfung der Funktionsfähigkeit eines Schaltungsentwurfs

Title (fr)

Méthode et appareil pour vérifier le fonctionnement de la conception d'un circuit

Publication

EP 1450278 B1 20130424 (EN)

Application

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- US 37355803 A 20030224

Abstract (en)

[origin: EP1450278A2] A method and apparatus are disclosed for debugging circuit designs having random access memory (RAM) therein. The circuit design is emulated on a hardware logic emulator or software simulator. The RAM can be rewound or reconstructed to a previous state, and then replayed. The RAM can also be reconstructed to a state in which the RAM was maintained at some point during a trace window.

IPC 8 full level

G06F 11/14 (2006.01); **G06F 17/50** (2006.01)

CPC (source: EP)

G06F 30/33 (2020.01); **G06F 30/331** (2020.01)

Citation (examination)

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- CLEARY J; GOMES F; UNGER B; XIAO ZHONGE; THUOT R: "Cost of state saving and rollback", PROCEEDINGS OF 8TH WORKSHOP ON PARALLEL AND DISTRIBUTED SIMULATION, 1994, Edinburgh, UK, pages 94 - 101

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