Title (en)

MEMORY CELL WITH A TRENCH TRANSISTOR

Title (de)

NICHTFLÜCHTIGE SPEICHERZELLE MIT GRABENTRANSISTOR

Title (fr)

CELLULE DE MEMOIRE COMPRENANT UN TRANSISTOR A TRANCHEE

Publication

EP 1456876 A2 20040915 (DE)

Application

EP 02791622 A 20021210

Priority

- DE 0204523 W 20021210
- DE 10162261 A 20011218
- US 2265401 A 20011218

Abstract (en)

[origin: WO03052812A2] The depth of the trench is optimized in such a way that the locations for the injection of electrons and holes correspond to the memory layer (11) disposed between the walls of the trench and the gate electrode (4) in defining layers (10,12). The junctions (14) where the doping of the source area (2) and the drain area (3) switches to the opposite polarity sign of the semiconductor body (1), and which define the channel area (5), abut against a curved area of the bottom (7) of the trench or a lower curved area of the side walls (6,8) of the trench.

IPC 1-7

H01L 21/336; H01L 27/115; H01L 21/8246; H01L 29/792

IPC 8 full level

H01L 21/8247 (2006.01); **H01L 29/423** (2006.01); **H01L 29/788** (2006.01); **H01L 29/792** (2006.01); **H10B 20/00** (2023.01); **H10B 69/00** (2023.01)

CPC (source: EP KR)

H01L 21/18 (2013.01 - KR); **H01L 29/792** (2013.01 - EP); **H10B 69/00** (2023.02 - EP); **H10B 99/00** (2023.02 - KR)

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