Title (en)

SCHOTTKY BARRIER CMOS DEVICE AND METHOD

Title (de)

CMOS BAUELEMENT MIT EINER SCHOTTKY-BARRIERE UND VERFAHREN

Title (fr)

DISPOSITIF CMOS A BARRIERE DE SCHOTTKY ET PROCEDE

Publication

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Application

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- US 38123802 P 20020516
- US 38123902 P 20020516
- US 38124002 P 20020516
- US 38132002 P 20020516
- US 38132102 P 20020516
- US 38865902 P 20020516
- US 38123702 P 20020516
- US 38123602 P 20020516
- US 38116202 P 20020516
- US 21544702 A 20020809
- US 23668502 A 20020906
- US 34259003 A 20030115
- US 44571103 P 20030207

Abstract (en)

[origin: WO03098693A2] A CMOS device and method of fabrication are disclosed. The present invention utilizes Schottky barrier contacts for source and/or drain contact fabrication within the context of a CMOS device and CMOS integrated circuits, to eliminate the requirement for halo/pocket implants, shallow source/drain extensions to control short channel effects, well implant steps, and complex device isolation steps. Additionally, the present invention eliminates the parasitic bipolar gain associated with CMOS device operation, reduces manufacturing costs, tightens control of device performance parameters, and provides for superior device characteristics as compared to the prior art. The present invention, in one embodiment, uses a silicide exclusion mask process to form the dual silicide Schottky barrier source and/or drain contact for the complimentary PMOS and NMOS devices forming the CMOS device.

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