

Title (en)
INTEGRATED CIRCUIT ARRANGEMENT

Title (de)
INTEGRIERTE SCHALTUNGSAORDNUNG

Title (fr)
ENSEMBLE CIRCUIT INTEGRE

Publication
EP 1522100 A1 20050413 (DE)

Application
EP 03764888 A 20030711

Priority
• DE 0302349 W 20030711
• DE 10231638 A 20020712

Abstract (en)
[origin: WO2004010501A1] The invention relates to an integrated circuit arrangement (150) comprising a monolithic serial inductance (125, 126). The integrated circuit arrangement (150) has an output circuit comprising at least one first output terminal (104, 108), at which a data signal can be provided and at least one first data output terminal (152, 154). At least one first serial inductance (125, 126) is connected between the output terminal(s) (104, 108) and the data output terminal(s) (152, 154).

IPC 1-7
H01L 23/66

IPC 8 full level
H01L 23/66 (2006.01); **H03F 3/45** (2006.01); **H03H 11/02** (2006.01); **H03H 7/01** (2006.01)

CPC (source: EP US)
H03F 3/45183 (2013.01 - EP US); **H01L 2924/0002** (2013.01 - EP US); **H03F 2203/45562** (2013.01 - EP US);
H03F 2203/45638 (2013.01 - EP US); **H03H 7/0115** (2013.01 - EP US)

Citation (search report)
See references of WO 2004010501A1

Designated contracting state (EPC)
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR

DOCDB simple family (publication)
WO 2004010501 A1 20040129; DE 10231638 A1 20040129; DE 10231638 B4 20110728; EP 1522100 A1 20050413;
US 2006232349 A1 20061019; US 7576619 B2 20090818

DOCDB simple family (application)
DE 0302349 W 20030711; DE 10231638 A 20020712; EP 03764888 A 20030711; US 52080505 A 20051013