Title (en)

ACCELERATION OF THE PROGRAMMING OF A MEMORY MODULE WITH THE AID OF A BOUNDARY SCAN (BSCAN) REGISTER

Title (de)

BESCHLEUNIGUNG DER PROGRAMMIERUNG EINES SPEICHERBAUSTEINS MIT HILFE EINES BOUNDARY SCAN (BSCAN)-REGISTERS

Title (fr)

ACCELERATION DE LA PROGRAMMATION D'UN MODULE DE MEMOIRE A L'AIDE D'UN REGISTRE A DECALAGE PERIPHERIQUE (BSCAN)

Publication

EP 1543528 A2 20050622 (DE)

Application

EP 03798062 A 20030903

Priority

- DE 0302932 W 20030903
- DE 10244977 A 20020926

Abstract (en)

[origin: WO2004029982A2] In order to program a memory module (104), some of its inputs (CS, OE, WR, ADDR, DATA) are stimulated via internal memory locations (103) of a so-called boundary scan (BSCAN) register (102) that is provided in the form of an IC or ASIC. In order to activate or deactivate a write operation, the control signal input (WR) of the memory module (104), said control signal input being responsible for generating a WRITE_ENABLE signal (301d), is controlled exclusively. The switching over of the WRITE_ENABLE signal (301d) from "LOW" to "HIGH" potential and vice versa thus ensues according to two JTAG instructions (WR_L, WR_H) of an instruction sequence (301a) that provides for the generation of a LOW or HIGH level at the setting signal input or resetting signal input of an update flip-flop (108) of the memory location (103) responsible for generating the WRITE_ENABLE signal. By appropriately modifying the control unit (106) and the BSCAN cell (103), which stimulates the WRITE_ENABLE signal (301d) at the WR input of the memory module (104), the programming can be accelerated without having to expand the interface between the control unit (106) and the BSCAN register (102) to the board and equipment level. In another embodiment of the invention, a control unit (106) automatically switches over the WRITE_ENABLE signal (301d) from "LOW" to "HIGH" potential or from HIGH to LOW potential at an appropriate or rather programmable point in time by setting or resetting the update flip-flop (108) of the memory location (103) responsible for generating the WRITE_ENABLE signal.

IPC 1-7

G11C 16/10

IPC 8 full level

G11C 29/30 (2006.01)

CPC (source: EP US)

G11C 29/30 (2013.01 - EP US); G11C 2029/3202 (2013.01 - EP US)

Citation (search report)

See references of WO 2004029982A2

Designated contracting state (EPC)

FR GB

DOCDB simple family (publication)

WO 2004029982 A2 20040408; **WO 2004029982 A3 20040527**; DE 10244977 A1 20040422; DE 10244977 B4 20040812; EP 1543528 A2 20050622; US 2006041801 A1 20060223; US 7173840 B2 20070206

DOCDB simple family (application)

DE 0302932 W 20030903; DE 10244977 A 20020926; EP 03798062 A 20030903; US 52933105 A 20050324