

Title (en)  
MEMORY CELL, MEMORY CELL ARRANGEMENT, STRUCTURING ARRANGEMENT AND METHOD FOR PRODUCTION OF A MEMORY CELL

Title (de)  
SPEICHERZELLE, SPEICHERZELLEN-ANORDNUNG, STRUKTURIER-ANORDNUNG UND VERFAHREN ZUM HERSTELLEN EINER SPEICHERZELLE

Title (fr)  
CELLULE DE MEMOIRE, ENSEMBLE DE CELLULES DE MEMOIRE, ENSEMBLE DE STRUCTURATION ET PROCEDE DE FABRICATION D'UNE CELLULE DE MEMOIRE

Publication  
**EP 1556893 A2 20050727 (DE)**

Application  
**EP 03778241 A 20031029**

Priority  
• DE 0303589 W 20031029  
• DE 10250834 A 20021031

Abstract (en)  
[origin: WO2004040644A2] The invention relates to a memory cell, memory cell arrangement, structuring arrangement and method for production of a memory cell. The memory cell has a vertical gate transistor and a memory capacitor, whereby the vertical gate transistor comprises a semiconducting nanostructure, grown on at least part of the memory capacitor.

IPC 1-7  
**H01L 21/8239**

IPC 8 full level  
**G11C 13/02** (2006.01); **H01L 21/8242** (2006.01); **H01L 27/108** (2006.01); **H01L 51/00** (2006.01); **H01L 51/05** (2006.01); **H01L 51/30** (2006.01)

CPC (source: EP US)  
**B82Y 10/00** (2013.01 - EP US); **G11C 13/0033** (2013.01 - EP US); **G11C 13/025** (2013.01 - EP US); **H10B 12/0383** (2023.02 - EP US); **H10B 12/395** (2023.02 - EP US); **H10K 19/10** (2023.02 - EP US); **G11C 2213/16** (2013.01 - EP US); **H10B 12/053** (2023.02 - EP US); **H10K 10/462** (2023.02 - EP US); **H10K 10/491** (2023.02 - EP US); **H10K 85/221** (2023.02 - EP US); **H10K 85/615** (2023.02 - EP US)

Citation (search report)  
See references of WO 2004040644A2

Designated contracting state (EPC)  
DE

DOCDB simple family (publication)  
**WO 2004040644 A2 20040513**; **WO 2004040644 A3 20040812**; DE 10250834 A1 20040519; EP 1556893 A2 20050727; US 2005276093 A1 20051215

DOCDB simple family (application)  
**DE 0303589 W 20031029**; DE 10250834 A 20021031; EP 03778241 A 20031029; US 11953105 A 20050429