

Title (en)

MONOLITHICALLY INTEGRATED VERTICAL PIN PHOTODIODE USED IN BICMOS TECHNOLOGY

Title (de)

MONOLITHISCH INTEGRIERTE VERTIKALE PIN-FOTODIODE IN BICMOS-TECHNOLOGIE

Title (fr)

PHOTODIODE PIN VERTICALE A INTEGRATION MONOLITHIQUE DANS LE CADRE DE LA TECHNOLOGIE BICMOS

Publication

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Application

EP 03767422 A 20031112

Priority

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- DE 10252878 A 20021112

Abstract (en)

[origin: WO2004044994A2] The invention relates to a monolithically integrated vertical pin photodiode which is produced according to BiCMOS technology and comprises a planar surface (30) facing the light ($h <$) and a rear face (31), and anode connections (A1, A2) located across p areas (20, 21) on a top face of the photodiode. An i zone of the pin photodiode is formed by combining a low doped first p-> epitaxial layer (10, d10) which has a maximum thickness of essentially 15nm and a doping concentration of less than 5×10^{14} cm $^{-3}$ and is placed on a particularly high doped p substrate (10), with a low doped second n-> epitaxial layer (9) that borders the first layer (10) and has a doping concentration ranging substantially between 10^{14} cm $^{-3}$ and 10^{15} cm $^{-3}$, an n+ cathode (K) of the pin photodiode being integrated into said second layer (9). p areas (20, 21) delimit the second n epitaxial layer (9) in a latent direction while another anode-connecting area (A3) of the pin diode is provided on the rear face (31) in addition to the anode connections (A1, A2).

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IPC 8 full level

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