Title (en)

A MULTI-LEVEL CONTROLLER SYSTEM

Title (de)

MEHRSTUFIGES STEUERSYSTEM

Title (fr)

SYSTEME D'UNITE DE COMMANDE MULTINIVEAU

Publication

EP 1565795 A1 20050824 (EN)

Application

EP 03768993 A 20031118

Priority

- US 0337136 W 20031118
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Abstract (en)

[origin: WO2004046834A1] A leveled system architecture (100) of figure 5 includes multiple level processors and/or controllers that control each other and ultimately the system components. The host level controller (56) includes a host processor, the level-1 controller (52) includes the master controller, the level-2 controller (54) includes four controllers (54a, 54b, 54c and 54d) and the level-3 controller includes one or more controllers that interface between the level-2 controllers and the system components. The motors, pumps, and the valves are controlled by the level-3 controllers, which are programmed in C and typically are not changeable the state records, which a processor engineer accesses to control the operation of the second and the level-2 controllers (52, 54), wherein the system executes a process by identifying a set of states to be executed, issuing state commands that need to be issued to execute the current state in the set of states.

IPC 1-7

G05B 11/01

IPC 8 full level

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CPC (source: EP US)

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