

Title (en)  
PIPELINE ACCELERATOR AND RELATED SYSTEM AND METHOD

Title (de)  
PIPELINE-BESCHLEUNIGER, SYSTEM UND VERFAHREN DAFÜR

Title (fr)  
ACCELERATEUR PIPELINE CON U POUR UNE ARCHITECTURE INFORMATIQUE AMELIOREE, ET SYSTEME ET PROCEDE ASSOCIES

Publication  
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Application  
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Abstract (en)  
[origin: WO2004042560A2] A peer-vector machine includes a host processor and a hardwired pipeline accelerator. The host processor executes a program, and, in response to the program, generates host data, and the pipeline accelerator generates pipeline data from the host data. Alternatively, the pipeline accelerator generates the pipeline data, and the host processor generates the host data from the pipeline data. Because the peer-vector machine includes both a processor and a pipeline accelerator, it can often process data more efficiently than a machine that includes only processors or only accelerators. For example, one can design the peer-vector machine so that the host processor performs decision-making and non-mathematically intensive operations and the accelerator performs non-decision-making and mathematically intensive operations. By shifting the mathematically intensive operations to the accelerator, the peer-vector machine often can, for a given clock frequency, process data at a speed that surpasses the speed at which a processor-only machine can process the data.

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IPC 8 full level  
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See references of WO 2004042562A2

Citation (examination)  
RICHARD R. ECKERT: "Microprogrammed versus hardwired control units: how computers really work", SIGCSE BULLETIN., vol. 20, no. 3, 1 September 1988 (1988-09-01), US, pages 13 - 22, XP055336753, ISSN: 0097-8418, DOI: 10.1145/51594.51598

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