

Title (en)

METHOD FOR MICROFABRICATING STRUCTURES USING SILICON-ON-INSULATOR MATERIAL

Title (de)

VERFAHREN ZUR MIKROHERSTELLUNG VON STRUKTUREN UNTER VERWENDUNG VON SILIZIUM-AUF-ISOLATOR-MATERIAL

Title (fr)

PROCEDE DE MICROUSINAGE DE STRUCTURES UTILISANT UN MATERIAU DE SILICIUM SUR ISOLANT

Publication

EP 1576650 A3 20051005 (EN)

Application

EP 03754388 A 20030815

Priority

- US 0325435 W 20030815
- US 40379602 P 20020815

Abstract (en)

[origin: WO2004017371A2] The invention provides a general fabrication method for producing MicroElectroMechanical Systems (MEMS) and related devices using Silicon-On-Insulator (SOI) wafer. The method includes providing an SOI wafer that has (i) a handle layer, (ii) a dielectric layer, and (iii) a device layer, wherein a mesa etch has been made on the device layer of the SOI wafer, providing a substrate, wherein a pattern has been etched onto the substrate, bonding the SOI wafer and the substrate together, removing the handle layer of the SOI wafer, removing the dielectric layer of the SOI wafer, then performing a structural etch on the device layer of the SOI wafer to define the device.

IPC 1-7

H01L 21/00

IPC 8 full level

B81C 3/00 (2006.01); **H01L 21/46** (2006.01)

CPC (source: EP)

B81C 1/00579 (2013.01); **B81C 3/001** (2013.01)

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR

DOCDB simple family (publication)

WO 2004017371 A2 20040226; **WO 2004017371 A3 20050818**; **WO 2004017371 A9 20040708**; AU 2003272215 A1 20040303; AU 2003272215 B2 20090910; AU 2009248425 A1 20100107; AU 2009248425 B2 20121220; EP 1576650 A2 20050921; EP 1576650 A3 20051005; EP 1576650 A4 20110615

DOCDB simple family (application)

US 0325435 W 20030815; AU 2003272215 A 20030815; AU 2009248425 A 20091210; EP 03754388 A 20030815