

Title (en)  
HARDWARE PARSER ACCELERATOR

Title (de)  
HARDWARE-ANALYSIERER-BESCHLEUNIGER

Title (fr)  
ACCELERATEUR D'ANALYSEUR MATERIEL

Publication  
**EP 1579320 A2 20050928 (EN)**

Application  
**EP 03809942 A 20031003**

Priority  

- US 0331314 W 20031003
- US 42177302 P 20021029
- US 42177402 P 20021029
- US 42177502 P 20021029
- US 33131502 A 20021231

Abstract (en)  
[origin: WO2004040446A2] Dedicated hardware is employed to perform parsing of documents such as XML"" documents in much reduced time while removing a substantial processing burden from the host CPU.The conventional use of a state table is divided into a character palette, a state table in abbreviated form, and a next state palette. The palettes may be implemented in dedicated high speed memory and a cache arrangement may be used to accelerate accesses to the abbreviated state table. Processing is performed in parallel pipelines which may be partially concurrent. Dedicated registers may be updated in parallel as well and strings of special characters of arbitrary length accommodated by a character palette skip feature under control of a flag bit to further accelerate parsing of a document.

IPC 1-7  
**G06F 9/45**

IPC 8 full level  
**G06F 9/45** (2006.01)

CPC (source: EP KR)  
**G06F 8/40** (2013.01 - KR); **G06F 40/205** (2020.01 - EP)

Citation (search report)  
See references of WO 2004040446A2

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DOCDB simple family (publication)  
**WO 2004040446 A2 20040513; WO 2004040446 A3 20040902**; AU 2003277249 A1 20040525; CA 2504652 A1 20040513; EP 1579320 A2 20050928; JP 2006505043 A 20060209; KR 20050072128 A 20050708

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