Title (en)

SRAM MEMORY CELL AND METHOD FOR COMPENSATING A LEAKAGE CURRENT FLOWING INTO THE SRAM MEMORY CELL

Title (de)

SRAM-SPEICHERZELLE UND VERFAHREN ZUM KOMPENSIEREN EINES IN DIE SRAM-SPEICHERZELLE FLIESSENDEN LECKSTROMS

Title (fr)

CELLULE DE MEMOIRE SRAM ET PROCEDE POUR COMPENSER UN COURANT DE FUITE CIRCULANT DANS LA CELLULE DE MEMOIRE SRAM

Publication

EP 1579456 A1 20050928 (DE)

Application

EP 03811723 A 20031024

Priority

- DE 0303551 W 20031024
- DE 10255102 A 20021126

Abstract (en)

[origin: DE10255102B3] The device is connected to at least one data line and has at least one memory node (K1,K2), at least one selection transistor (M5) connected to the first node, a first data line (BL), a first word line (WL1) and an arrangement (M7) for adapting the leakage current that causes a total leakage current from at least one bit line (BL) into the cell independent of the memory state of the cell, especially in the non-selected state.

IPC 1-7

G11C 11/412; G11C 11/419

IPC 8 full level

G11C 7/02 (2006.01); **G11C 11/412** (2006.01); **G11C 11/419** (2006.01); **H01L 27/11** (2006.01)

CPC (source: EP US)

G11C 11/412 (2013.01 - EP US)

Citation (search report)

See references of WO 2004049348A1

Citation (examination)

- JP H11260063 A 19990924 - HITACHI LTD
- US 5673230 A 19970930 - KURIYAMA HIROTADA [JP]

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

DE 10255102 B3 20040429; CN 100557707 C 20091104; CN 1717747 A 20060104; EP 1579456 A1 20050928; JP 2006507617 A 20060302; US 2005281109 A1 20051222; US 7504695 B2 20090317; WO 2004049348 A1 20040610

DOCDB simple family (application)

DE 10255102 A 20021126; CN 200380104256 A 20031024; DE 0303551 W 20031024; EP 03811723 A 20031024; JP 2004554189 A 20031024; US 13729405 A 20050525