Title (en)

CARRY-RIPPLE ADDER

Title (de)

CARRY-RIPPLE ADDIERER

Title (fr)

ADDITIONNEUR PAR REPORT EN CASCADE

Publication

EP 1593035 A2 20051109 (DE)

Application

EP 04706161 A 20040129

Priority

- EP 2004000796 W 20040129
- DE 10305849 A 20030212

Abstract (en)

[origin: DE10305849B3] The carry-ripple adder (10) has 3 inputs (I0,I1,I2) for reception of 3 input bits of similar value, 2 further carry inputs (CI1,CI2) for reception of carry bits of similar value, an output (S) for delivery of a calculated sum bit and 2 ouputs (CO1,CO2 for delivery of carry bits with a higher value than the calculated sum bit. A pre-charge input may be provided for controlling an integrated pre-charge logic stage.

IPC 1-7

G06F 7/50

IPC 8 full level

G06F 7/509 (2006.01); **G06F 7/50** (2006.01); **G06F 7/60** (2006.01); G06F 7/53 (2006.01)

IPC 8 main group level

H04B (2006.01)

CPC (source: EP US)

G06F 7/607 (2013.01 - EP US); G06F 7/509 (2013.01 - EP US); G06F 7/5318 (2013.01 - EP US); G06F 2207/3872 (2013.01 - EP US)

Citation (search report)

See references of WO 2004073171A2

Citation (examination)

- US 5805491 A 19980908 - BECHADE ROLAND A [US]
- US 2002070781 A1 20020613 - VANGAL SRIRAM R [US], et al

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

DE 10305849 B3 20040715; CN 100541417 C 20090916; CN 1748200 A 20060315; EP 1593035 A2 20051109; JP 2006517700 A 20060727; JP 4157141 B2 20080924; US 2006294178 A1 20061228; WO 2004073171 A2 20040826; WO 2004073171 A3 20050310

DOCDB simple family (application)

DE 10305849 A 20030212; CN 200480003578 A 20040129; EP 04706161 A 20040129; EP 2004000796 W 20040129; JP 2006500019 A 20040129; US 20344505 A 20050812