

Title (en)
SEMICONDUCTOR CHIP ARRANGEMENT WITH ROM

Title (de)
HALBLEITERCHIPANORDNUNG MIT ROM

Title (fr)
CONFIGURATION DE PUCES A SEMI-CONDUCTEURS COMPRENANT UNE MEMOIRE MORTE (ROM)

Publication
EP 1597734 A1 20051123 (DE)

Application
EP 04710779 A 20040213

Priority
• DE 2004000269 W 20040213
• DE 10308323 A 20030226

Abstract (en)
[origin: WO2004077450A1] A structured junction plane between two semiconductors produced in face-to-face technology is structured in first terminal faces (7) and second terminal faces (8) and alternatively in conductor strips (9) linked with one of the terminal faces. The conductor strips (9) are linked with a read-out circuit in one of the semiconductor chips via connections (11). This arrangement can be operated as ROM.

IPC 1-7
G11C 17/10; **H01L 25/065**

IPC 8 full level
G11C 17/10 (2006.01); **H01L 25/065** (2006.01); **H01L 23/528** (2006.01)

CPC (source: EP US)
G11C 17/10 (2013.01 - EP US); **H01L 25/0657** (2013.01 - EP US); **H01L 23/5286** (2013.01 - EP US); **H01L 2225/06527** (2013.01 - EP US); **H01L 2225/06555** (2013.01 - EP US); **H01L 2924/0002** (2013.01 - EP US)

Citation (search report)
See references of WO 2004077450A1

Designated contracting state (EPC)
DE FR

DOCDB simple family (publication)
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