Title (en)

FERROELECTRIC MEMORY DEVICE

Title (de)

FERROELEKTRISCHER SPEICHERBAUSTEIN

Title (fr)

MEMOIRE FERROELECTRIQUE

Publication

EP 1631964 A2 20060308 (EN)

Application

EP 04736356 A 20040608

Priority

- JP 2004008288 W 20040608
- JP 2003164141 A 20030609

Abstract (en)

[origin: WO2004109705A2] A ferroelectric memory device includes a memory cell array having memory cells arranged in a matrix form. Each of the memory cells includes a cell transistor and a ferroelectric capacitor. It further includes a first dummy bit line arranged outside a bit line arranged on an end portion of the memory cell array, and separated from the bit line arranged on the end portion of the memory cell array with an interval which is the same as a pitch between the bit lines in the memory cell array, the first dummy bit line having the same width as the bit line, and a first dummy memory cell connected to the first dummy bit line and including a cell transistor and a ferroelectric capacitor.

IPC 1-7

G11C 11/22

IPC 8 full level

G11C 11/22 (2006.01); **H01L 21/8246** (2006.01); **H01L 27/10** (2006.01); **H01L 27/105** (2006.01)

CPC (source: EP KR)

G11C 5/063 (2013.01 - KR); **G11C 7/06** (2013.01 - KR); **G11C 7/18** (2013.01 - KR); **G11C 11/22** (2013.01 - EP); **G11C 11/221** (2013.01 - KR); **G11C 11/2273** (2013.01 - KR)

Citation (search report)

See references of WO 2004109705A2

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