

Title (en)  
DELAY-FAULT TESTING METHOD, RELATED SYSTEM AND CIRCUIT

Title (de)  
VERZÖGERUNGSFEHLER-TESTVERFAHREN, ZUGEHÖRIGES SYSTEM UND SCHALTUNG

Title (fr)  
PROCEDE, SYSTEME ET CIRCUIT DE CONTROLE D'ERREURS DE RETARD

Publication  
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Application  
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Abstract (en)  
[origin: WO2004106958A1] A testing approach involves selective application of clock signals to target circuitry. In an example embodiment (300), a target circuit (332) having logic circuitry that processes data in response to an operational clock signal (308) having at least one clock period, is analyzed for delay faults. Test signals are applied to the logic circuitry while the logic circuitry is clocked with a high-speed test clock (309) having several clock-state transitions that occur during at least one clock period of the operational clock (308). An output from the logic circuitry is analyzed for its state (e.g., as affected by delay in the circuitry). Delay faults are detected as a difference in state of the output of the logic circuitry. With this approach, circuits are tested using conventional testers (340) that operate at normal (e.g., slow) speeds while selectively clocking selected portions of the circuit at higher speeds for detecting speed-related faults therein.

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