Title (en)

METHOD AND CIRCUIT ARRANGEMENT FOR SIMULATING PIXEL AND SUB-PIXEL DEFECTS THAT OCCUR IN MATRIX-ADDRESSED DISPLAYS

Title (de)

VERFAHREN UND SCHALTUNGSANORDNUNG ZUR SIMULATION VON BEI MATRIXADRESSIERTEN DISPLAYS AUFTRETENDEN PIXEL- UND SUBPIXELDEFEKTEN

Title (fr)

PROCEDE ET CIRCUITERIE POUR SIMULER DES DEFAUTS AU NIVEAU PIXEL ET SOUS-PIXEL APPARAISSANT DANS DES AFFICHAGES A ADRESSAGE MATRICIEL

Publication

EP 1636777 A1 20060322 (DE)

Application

EP 04722816 A 20040324

Priority

- EP 2004003097 W 20040324
- DE 10314268 A 20030329

Abstract (en)

[origin: DE10314268B3] The pixel and sub-pixel defect simulation method uses a programmable pixel defect simulation unit (3) for replacing the red-green-blue signal (10) obtained from the video image data stream with a modified red-green-blue signal (11) which simulates pixel or sub-pixel defects, the timing and duration of the signal replacement controlled for obtaining the pixel or sub-pixel defect at a required point on the display screen. An independent claim for a circuit device for simulation of pixel and sub-pixel defects for a matrix-addressed display is also included.

IPC 1-7

G09G 3/20

IPC 8 full level

G09G 3/20 (2006.01); G09G 3/00 (2006.01)

CPC (source: EP)

G09G 3/20 (2013.01); G09G 3/006 (2013.01); G09G 2330/10 (2013.01)

Citation (search report)

See references of WO 2004088621A1

Citation (examination)

- JP H06201516 A 19940719 - SONY CORP
- JP H09257639 A 19971003 - FUJITSU LTD
- US 5986697 A 19991116 - CAHILL III BENJAMIN M [US]

Designated contracting state (EPC)

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DOCDB simple family (publication)

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DE 10314268 A 20030329; CN 200480008696 A 20040324; EP 04722816 A 20040324; EP 2004003097 W 20040324; JP 2006504832 A 20040324