

Title (en)

MASTER LATCH CIRCUIT WITH SIGNAL LEVEL DISPLACEMENT FOR A DYNAMIC FLIP-FLOP

Title (de)

MASTER-LATCHSCHALTUNG MIT SIGNALPEGELVERSCHIEBUNG FÜR EIN DYNAMISCHES FLIP-FLOP

Title (fr)

CIRCUIT DE VERROUILLAGE MAITRE A DECALAGE DE NIVEAU DE SIGNAL POUR UNE BASCULE DYNAMIQUE

Publication

**EP 1665529 A2 20060607 (DE)**

Application

**EP 04764805 A 20040903**

Priority

- EP 2004009853 W 20040903
- DE 10343565 A 20030919

Abstract (en)

[origin: DE10343565B3] The master latch circuit (10) has a signal delay circuit (13) for delaying a received clock signal (Clk) and a circuit node (14) which is charged to an operating voltage during a charging phase and discharged in dependence on an applied data signal (D) in an evaluation phase, the circuit node coupled to a reference potential via at least one capacitor (15).

IPC 1-7

**H03K 3/037**; **H03K 3/356**

IPC 8 full level

**H03K 3/037** (2006.01); **H03K 3/356** (2006.01)

CPC (source: EP US)

**H03K 3/037** (2013.01 - EP US); **H03K 3/356121** (2013.01 - EP US)

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DOCDB simple family (publication)

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