Title (en)

METHOD AND APPARATUS FOR A VARIABLE PROCESSING PERIOD IN AN INTEGRATED CIRCUIT

Title (de)

VERFAHREN UND VORRICHTUNG FÜR EINE VARIABLE VERARBEITUNGSPERIODE IN EINER INTEGRIERTEN SCHALTUNG

Title (fr)

PROCEDE ET APPAREIL A PERIODE DE TRAITEMENT VARIABLE DANS UN CIRCUIT INTEGRE

Publication

EP 1676192 A4 20081210 (EN)

Application

EP 04795572 A 20041015

Priority

- US 2004034429 W 20041015
- FR 0312485 A 20031024
- US 86168204 A 20040604

Abstract (en)

[origin: WO2005043299A2] The invention is a system for modifying the processing period in a digital logic module. The invention comprises the following. A processing circuit is configured to receive an input in order to create an output. A controller is coupled to the processing circuit and is configured to track L manipulations, wherein L is an integer. The controller is further configured to send a select signal to the processing circuit and to cause the processing circuit to manipulate the input over N clock cycles. N is an integer and N is less than or equal to L. N varies over the plurality of processing time periods. An output port is coupled to the processing circuit and is configured to convey the output.

IPC 8 full level

G06F 1/00 (2006.01)

IPC 8 main group level

G06F (2006.01)

CPC (source: EP)

G06F 21/72 (2013.01); **G06F 21/755** (2017.07)

Citation (search report)

- [Y] US 2002124178 A1 20020905 - KOCHER PAUL C [US], et al
- [A] US 2001038637 A1 20011108 - REINER ROBERT [DE], et al
- [YX] KAPS J, PAAR C: "Fast DES Implementations for FPGAs and its Application to a Universal Key-Search Machine", LECTURE NOTES IN COMPUTER SCIENCE, vol. 1556, 1999, pages 234 - 247, XP002377668
- See references of WO 2005043299A2

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

WO 2005043299 A2 20050512; **WO 2005043299 A3 20060928**; EP 1676192 A2 20060705; EP 1676192 A4 20081210

DOCDB simple family (application)

US 2004034429 W 20041015; EP 04795572 A 20041015