

Title (en)

METHOD AND DEVICE FOR SECURE, INSULATED AND ELECTRICALLY CONDUCTIVE ASSEMBLING OF TREATED SEMICONDUCTOR WAFERS

Title (de)

FESTES ISOLIERENDES UND ELEKTRISCH LEITENDES VERBINDEN PROZESSIERTER HALBLEITERSCHEIBEN

Title (fr)

PROCEDE ET DISPOSITIF POUR ASSEMBLER SOLIDEMENT, DE MANIERE ISOLANTE ET ELECTROCONDUCTRICE, DES PLAQUETTES DE SEMICONDUCTEURS TRAITEES

Publication

EP 1678074 A1 20060712 (DE)

Application

EP 04802660 A 20041029

Priority

- DE 2004002413 W 20041029
- DE 10350460 A 20031029

Abstract (en)

[origin: WO2005042401A1] The invention concerns a method and a device for assembling treated semiconductor wafers (1, 2), for obtaining not only a secure assembly, but an electrical connection (5) between the semiconductor wafers or between the electronic structures (3) comprising the latter as well. The invention is characterized in that the secure assembly is produced by means of structured intermediate glass layers (6; 6a), with low melting point, acting as insulating layers, and the electrical connection is produced by means of an electroconductive sealing glass (5).

IPC 1-7

B81B 7/00

IPC 8 full level

B81B 7/00 (2006.01); **B81C 1/00** (2006.01)

CPC (source: EP US)

B81C 1/00301 (2013.01 - EP US); **B81B 2207/093** (2013.01 - EP US); **B81C 2203/019** (2013.01 - EP US)

Citation (search report)

See references of WO 2005042401A1

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PL PT RO SE SI SK TR

DOCDB simple family (publication)

WO 2005042401 A1 20050512; CA 2543736 A1 20050512; CN 1874956 A 20061206; DE 10350460 A1 20050630; DE 10350460 B4 20060713; DE 112004002626 D2 20060921; EP 1678074 A1 20060712; JP 2007510295 A 20070419; US 2008029878 A1 20080207; US 8129255 B2 20120306

DOCDB simple family (application)

DE 2004002413 W 20041029; CA 2543736 A 20041029; CN 200480031977 A 20041029; DE 10350460 A 20031029; DE 112004002626 T 20041029; EP 04802660 A 20041029; JP 2006537055 A 20041029; US 59530304 A 20041029