

Title (en)

INTEGRATED CIRCUIT COMPRISING Laterally Dielectrically Isolated Active Regions Above an Electrically Contacted Buried Material, and Method for Producing the Same

Title (de)

Integrierte Schaltung mit lateraler dielektrischer Isolation aktiver Bereiche über elektrisch kontaktiertem vergrabenen Material und Herstellungsverfahren

Title (fr)

Circuit Integre Pourvu de Zones Actives a Isolation Dielectrique Laterale sur un Matériau Enfoui de Contact Electrique et son Procédé de Production

Publication

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Application

EP 05706945 A 20050121

Priority

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Abstract (en)

[origin: WO2005071737A1] The invention relates to an integrated circuit comprising a first layer (12) consisting of an active semiconductor material extending along a first side (14) of a buried layer (16), and trench structures (18, 38) that cut through the layer (12) of active semiconductor material and have dielectric wall regions (42, 44). Said dielectric wall regions (42, 44) electrically isolate partial regions (52, 54, 56) of the layer (12) of active semiconductor material in the lateral direction, and the trench structures (18, 38) also comprise first inner regions (46) that are filled with an electroconductive material and electroconductively contact the buried layer (16). The integrated circuit is characterised in that first wall regions (42) of the trench structures (18, 38) completely cut through the buried layer (16), and second wall regions (44) of the trench structures (18, 38) protrude into the buried layer (16), without completely cutting the same. The invention also relates to a method for producing one such integrated circuit.

IPC 8 full level

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CPC (source: EP US)

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