Title (en)
VERTICAL GATE CMOS WITH LITHOGRAPHY-INDEPENDENT GATE LENGTH

Title (de)
VERTIKAL-GATE-CMOS MIT LITHOGRAPHIEUNABHÄNGIGER GATELÄNGE

Title (fr)
CMOS A GRILLE VERTICALE PRESENTANT UNE LONGUEUR DE GRILLE INDEPENDANTE DE LA LITHOGRAPHIE

Publication
**EP 1709680 A4 20080702 (EN)**

Application
**EP 05705754 A 20050118**

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• US 76187604 A 20040121

Abstract (en)
[origin: WO2005072154A2] Formation of elements of a vertical transistor is described, particularly, a gate (1905)- source (1901) - drain (1903) arrangement of a CMOS transistor. Vertical transistors are used frequently in the integrated circuit art. Accordingly, improved methods for their formation, which are not limited by constraints of photolithography, have great utility and importance. Those of skill in the art will appreciate that the techniques described may be used to fabricate other types of devices as well. For example, junctions of a bipolar transistor (as well as other device junction types) may be fabricated using the methods described herein.

IPC 8 full level
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CPC (source: EP)
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Citation (search report)
• [AX] US 2002098657 A1 20020725 - ALAVI MOHSEN [US], et al
• [A] US 2001017392 A1 20010830 - COMFORT JAMES HARTFIEL [US], et al
• [A] US 5599724 A 19970204 - YOSHIDA TAKESHI [JP]
• [A] US 5402002 A 19950328 - MEISTER THOMAS [DE], et al
• See references of WO 2005072154A2

Designated contracting state (EPC)
DE FR GB IT

DOCDB simple family (publication)
**WO 2005072154 A2 20050811**; **WO 2005072154 A3 20051208**; CN 100442477 C 20081210; CN 1910748 A 20070207; EP 1709680 A2 20061011; EP 1709680 A4 20080702; TW 200531215 A 20050916

DOCDB simple family (application)
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