

Title (en)

METHOD AND INTEGRATED SWITCHING CIRCUIT FOR INCREASING THE IMMUNITY TO INTERFERENCE

Title (de)

VERFAHREN UND INTEGRIERTER SCHALTKREIS ZUR ERHUNG DER STÖRUFESTIGKEIT

Title (fr)

PROCEDE ET CIRCUIT INTEGRE PERMETTANT D'AMELIORER LA RESISTANCE AUX INTERFERENCES

Publication

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Application

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Priority

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Abstract (en)

[origin: WO2005081107A1] The invention relates to a method for increasing the immunity to interference of an integrated switching circuit (16). According to said method, error signals are transmitted between at least one microprocessor chip or multiple microcontroller (1) and at least one additional component (2) in the form of one or more such error signals. A minimum pulse length, which is independent of the clock pulse frequency of the microprocessor or microprocessors, is defined for said transmission. A signal on an error line with a specific pulse length that is in excess of said minimum length is interpreted as an error. The invention also relates to an integrated switching circuit, which is configured in particular to carry out the aforementioned method and comprises at least one microprocessor chip or multiple microcontroller (1) and at least one additional component (2), which contains in particular separate power components and one or more pulse spreading units and/or signal delay units for the sequential emission of error pulses (6, 6') via at least one error line (3, 4)

IPC 8 full level

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CPC (source: EP KR US)

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