Title (en)

On chip real time FPN correction without imager size memory

Title (de)

Echtzeit-FPN-Korrektur auf einem Chip ohne Speicher in ganzer Bildspeichergrösse

Title (fr)

Correction de FPN en temps réel sur une puce sans avoir de mémoire ayant la taille du dispositif de prise d'images

Publication

EP 1725019 A2 20061122 (EN)

Application

EP 06392007 A 20060517

Priority

US 13276905 A 20050519

Abstract (en)

A circuit and method for correcting pixel output signals for fixed pattern noise. Pixels in a selected row of pixels are read after an integration period and the resulting signals are stored in a first sample and hold circuit for each column. The pixels in the selected row are then reset and immediately read again and the resulting signals are stored in a second sample and hold circuit for each column. The signals in the second sample and hold circuits are subtracted from the signals in the first sample and hold circuits to produce signals related to the light seen by the pixels in the selected row corrected for fixed pattern noise. The output of the first sample and hold circuits and second sample and hold circuits can be connected to a subtraction unit and sequentially activated so that a single subtraction unit is required for the entire imager. The output of the subtraction unit can connected to a buffer thereby storing signals corrected for fixed pattern noise in the buffer using only a single subtraction unit and avoiding the need for a large memory to store dark pixel signals.

IPC 8 full level

H04N 3/15 (2006.01)

CPC (source: EP US)

H04N 25/616 (2023.01 - EP US); **H04N 25/677** (2023.01 - EP US); **H04N 25/78** (2023.01 - EP)

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR

Designated extension state (EPC)

AL BA HR MK YU

DOCDB simple family (publication)

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