Title (en)
   Hardware concept for a reset circuit

Title (de)
   Hardwarekonzept einer Reset-Schaltung

Title (fr)
   Concept matériel d'un circuit de réinitialisation

Publication
   EP 1727049 A3 20090617 (DE)

Application
   EP 06001920 A 20060131

Priority
   DE 102005024550 A 20050528

Abstract (en)
   [origin: EP1727049A2] Circuit arrangement has at least a transistor input stage (3) and a trip stage (4), which in each case comprises an output
   and at least one input, whereby the transistor input stage is connected with the status output of the microprocessor (1) or microcontroller (1). The
   transistor input stage changes a clocked status signal into an output signal, which corresponds to the first condition. An unclocked status signal
   changes into an output signal, which corresponds the second condition. The first input (E 1) of the trip stage is subjected with the output signal. As a
   result of the collection of the condition change at the first output (A 1) of the trip stage, a reset signal is generated at the first output of the trip stage.

IPC 8 full level
   G06F 11/00 (2006.01); G06F 1/24 (2006.01)

CPC (source: EP)
   G06F 1/24 (2013.01); **G06F 11/0757** (2013.01)

Citation (search report)
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Designated contracting state (EPC)
   AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR

Designated extension state (EPC)
   AL BA HR MK YU

DOCDB simple family (publication)
   EP 1727049 A2 20061129; **EP 1727049 A3 20090617**; DE 102005024550 A1 20061130

DOCDB simple family (application)
   EP 06001920 A 20060131; DE 102005024550 A 20050528