Title (en)

PROGRAMMABLE CLOCK GENERATION

Title (de)

PROGRAMMIERBARE TAKTERZEUGUNG

Title (fr)

GENERATION D'HORLOGE PROGRAMMABLE

Publication

EP 1728139 A2 20061206 (EN)

Application

EP 05708859 A 20050228

Priority

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Abstract (en)

[origin: WO2005088421A2] A mechanism for generating a clock signal for an integrated circuit, or part of one, so that the frequency thereof can be safely changed continuously (i.e. with a gradual frequency change) without spurious signals or glitches being created on the clock output line. A electronic device according to an exemplary embodiment, comprises a multiplexer (10) having two input signals, the second of which is a delayed version of the first, created by feeding the input to the multiplexer (10) via a set of generic combinatorial delay elements (12) and the multiplexer output id fed to the output (Out) via an inverter (14). The element further comprises a D-type flip-flop (16) having as its "D" input a programming signal (Fk), and the two outputs "Q" and "Qn" from the D-type flip-flop provided respective drive signals to the multiplexer (10). The delay of the output signal (Out) with respect to the input signal (In) depends on the value of the programming signal (Fk), which is synchronized on the rising edge of the local clock (sync_ck).

IPC 8 full level

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CPC (source: EP)

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