Title (en)

DUAL-PROCESSOR COMPLEX DOMAIN FLOATING-POINT DSP SYSTEM ON CHIP

Title (de)

CHIP-DOPPELPROZESSOR-GLEITKOMMA-DIGITALSIGNALPROZESSORSYSTEM FÜR KOMPLEXE DOMÄNEN

Title (fr)

SYSTEME SUR PUCE A PROCESSEUR DE SIGNAUX NUMERIQUES A VIRGULE FLOTTANTE COMPRENANT UN DOMAINE COMPLEXE A PROCESSEUR DOUBLE

Publication

EP 1728171 A2 20061206 (EN)

Application

EP 05724719 A 20050307

Priority
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- US 98652804 A 20041110

Abstract (en)

[origin: WO2005103922A2] A system for digital signal processing, configured as a system on chip (SoC) (102), combines a microprocessor core (106) and digital signal processor (DSP) core (108) with floating-point data processing capability. The DSP core (108) can perform operations on floating-point data in a complex domain and is capable of producing real and imaginary arithmetic results simultaneously. This capability allows a single-cycle execution of, for example, FFT butterflies, complex domain simultaneous addition and subtraction, complex multiply accumulate (MULACC), and real domain dual multiply-accumulators (MACs). The SoC (102) may be programmed entirely from a microprocessor programming interface (140), using calls from a DSP library to execute DSP functions. The cores (106, 108) may also be programmed separately. Capability for programming and simulating the entire SoC (102) are provided by a seprate programming environment. The SoC (102) may have heterogeneous processing cores in which either processing core may act as master or slave, or both cores may operate simultaneously and independently.

IPC 8 full level

G06F 7/38 (2006.01); **G06F 7/57** (2006.01); **G06F 15/00** (2006.01)

CPC (source: EP US)

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See references of WO 2005103922A2

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WO 2005103922 A2 20051103; **WO 2005103922 A3 20070329**; **WO 2005103922 A8 20070726**; EP 1728171 A2 20061206; US 2007168908 A1 20070719

DOCDB simple family (application)

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