

Title (en)

Method for forming a semiconductor memory device with a recessed gate

Title (de)

Verfahren zur Herstellung einer Halbleiterspeichervorrichtung mit einem versenkten Gate

Title (fr)

Procédé de fabrication d'un dispositif de mémoire semiconducteur avec porte encastrée

Publication

EP 1729338 A3 20090415 (EN)

Application

EP 06010091 A 20060516

Priority

US 14165605 A 20050531

Abstract (en)

[origin: EP1729338A2] Method for forming a semiconductor memory device with a recessed gate. A substrate (208), having a plurality of deep trench capacitors (206) therein, is provided wherein upper portions of the deep trench capacitor devices are revealed. Spacers (226) on sidewalls of the upper portions of the deep trench capacitors are formed to form a predetermined region surrounded by the deep trench capacitor devices. The predetermined region of the substrate is etched using the spacers and the upper portions of the deep trench capacitors serve as a mask to form a recess (228), and a recessed gate (230,232) is formed in the recess.

IPC 8 full level

H10B 12/00 (2023.01)

CPC (source: EP KR US)

H01L 21/18 (2013.01 - KR); **H10B 12/053** (2023.02 - EP US); **H10B 12/34** (2023.02 - EP US); **H10B 12/37** (2023.02 - EP US);
H10B 12/488 (2023.02 - EP US)

Citation (search report)

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Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR

Designated extension state (EPC)

AL BA HR MK YU

DOCDB simple family (publication)

EP 1729338 A2 20061206; **EP 1729338 A3 20090415**; **EP 1729338 B1 20160706**; CN 100388464 C 20080514; CN 1873948 A 20061206;
JP 2006339648 A 20061214; JP 4427037 B2 20100303; KR 100749035 B1 20070814; KR 20060124597 A 20061205;
TW 200642043 A 20061201; TW I302363 B 20081021; US 2006270149 A1 20061130; US 7316952 B2 20080108

DOCDB simple family (application)

EP 06010091 A 20060516; CN 200610087663 A 20060531; JP 2006150946 A 20060531; KR 20060047988 A 20060529;
TW 95118105 A 20060522; US 14165605 A 20050531