Title (en)

Method and Circuit for interpolating an Encoder Output

Title (de)

Verfahren und Schaltungsanordnung zur Interpolation des Ausgangssignals eines Kodierers

Title (fr)

Procédé et circuit d'interpolation de sortie d'un encodeur

Publication

EP 1752740 B1 20081203 (EN)

Application

EP 06118085 A 20060728

Priority

JP 2005233558 A 20050811

Abstract (en)

[origin: EP1752740A1] Two-phase sinusoidal signals QA, QB output from an encoder are interpolated by sample-and-hold (S/H) circuits and A/D conversion (ADC) circuits, and data D is output in accordance with a data request signal RQ from exterior. For this interpolation of encoder output, a direction discrimination up/down counter is arranged near a two-phase square-wave uniform pulse generating circuit, and the data D is latched and output using a signal which is obtained by delaying the data request signal RQ. This can reduce synchronization errors between the data request signal RQ from exterior and the interpolated data, with an improvement in dynamic precision.

IPC 8 full level

G01D 5/244 (2006.01)

CPC (source: EP US)

G01D 5/24404 (2013.01 - EP US); **H03M 1/207** (2013.01 - EP US); H03M 1/303 (2013.01 - EP US)

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DOCDB simple family (publication)

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