Title (en)

METHOD AND APPARATUS FOR DESIGNING INTEGRATED CIRCUIT LAYOUTS

Title (de)

VERFAHREN UND VORRICHTUNG ZUM ENTWURF VON LAYOUTS INTEGRIERTER SCHALTUNGEN

Title (fr)

PROCEDE ET APPAREIL POUR LA CONCEPTION DE TOPOLOGIES DE CIRCUITS INTEGRES

Publication

EP 1759321 A4 20091028 (EN)

Application

EP 05740549 A 20050429

Priority

- US 2005015024 W 20050429
- US 83658104 A 20040501
- US 83658204 A 20040501

Abstract (en)

[origin: WO2005109256A2] A method for modifying an IC layout using a library of pretabulated models, each model containing an environment with a feature, one or more geometries, and a modification to the feature that is calculated to produce a satisfactory feature on a wafer. The model may also contain a simulation of the environment reflecting no processing variations and/or a re-simulation of the environment reflecting one or more processing variations. The model may also contain data describing an electrical characteristic of the environment as a function of one or more process variations and/or data describing an adjustment equation that uses geometry coverage percentages of particular areas in the layout to determine an adjustment to the modification. In some embodiments, an upper layout for an upper of an IC are modified using information (such a density map) relating to a lower layout for a lower layer of the IC.

IPC 8 full level

G06F 17/50 (2006.01); G03F 1/36 (2012.01)

CPC (source: EP)

G06F 30/39 (2020.01); G03F 1/36 (2013.01)

Citation (search report)

- [X] US 2004058255 A1 20040325 - JESSEN SCOTT [US], et al
- [X] US 2003229412 A1 20031211 - WHITE DAVID [US], et al
- See references of WO 2005109257A2

Designated contracting state (EPC)

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DOCDB simple family (publication)

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US 2005014983 W 20050429; EP 05740549 A 20050429; EP 05740554 A 20050429; JP 2007511456 A 20050429; JP 2007511459 A 20050429; US 2005015024 W 20050429