Title (en)

METHOS AND APPARATUS FOR DESIGNING INTEGRATED CIRCUIT LAYOUTS

Title (de)

VERFAHREN UND VORRICHTUNGEN ZUM ENTWERFEN VON LAYOUTS INTEGRIERTER SCHALTUNGEN

Title (fr)

PROCEDES ET DISPOSITIF POUR LA CONCEPTION DE TOPOLOGIES DE CIRCUITS INTEGRES

Publication

EP 1759322 A2 20070307 (EN)

Application

EP 05740554 A 20050429

Priority

- US 2005014983 W 20050429
- US 83658104 A 20040501
- US 83658204 A 20040501

Abstract (en)

[origin: WO2005109256A2] A method for modifying an IC layout using a library of pretabulated models, each model containing an environment with a feature, one or more geometries, and a modification to the feature that is calculated to produce a satisfactory feature on a wafer. The model may also contain a simulation of the environment reflecting no processing variations and/or a re-simulation of the environment reflecting one or more processing variations. The model may also contain data describing an electrical characteristic of the environment as a function of one or more process variations and/or data describing an adjustment equation that uses geometry coverage percentages of particular areas in the layout to determine an adjustment to the modification. In some embodiments, an upper layout for an upper of an IC are modified using information (such a density map) relating to a lower layout for a lower layer of the IC.

IPC 8 full level

G06F 17/50 (2006.01); G03F 1/36 (2012.01)

CPC (source: EP)

G06F 30/39 (2020.01); G03F 1/36 (2013.01)

Designated contracting state (EPC)

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU MC NL PL PT RO SE SI SK TR

DOCDB simple family (publication)

WO 2005109256 A2 20051117; **WO 2005109256 A3 20060504**; EP 1759321 A2 20070307; EP 1759321 A4 20091028; EP 1759322 A2 20070307; EP 1759322 A4 20080312; JP 2007535715 A 20071206; JP 2007538272 A 20071227; JP 5147391 B2 20130220; WO 2005109257 A2 20051117; WO 2005109257 A3 20051215

DOCDB simple family (application)

US 2005014983 W 20050429; EP 05740549 A 20050429; EP 05740554 A 20050429; JP 2007511456 A 20050429; JP 2007511459 A 20050429; US 2005015024 W 20050429