Title (en)

METHOS AND APPARATUS FOR DESIGNING INTEGRATED CIRCUIT LAYOUTS

Title (de)

VERFAHREN UND VORRICHTUNGEN ZUM ENTWERFEN VON LAYOUTS INTEGRIERTER SCHALTUNGEN

Title (fr)

PROCEDES ET DISPOSITIF POUR LA CONCEPTION DE TOPOLOGIES DE CIRCUITS INTEGRES

Publication

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Application

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Abstract (en)

[origin: WO2005109256A2] A method for modifying an IC layout using a library of pretabulated models, each model containing an environment with a feature, one or more geometries, and a modification to the feature that is calculated to produce a satisfactory feature on a wafer. The model may also contain a simulation of the environment reflecting no processing variations and/or a re-simulation of the environment reflecting one or more processing variations. The model may also contain data describing an electrical characteristic of the environment as a function of one or more process variations and/or data describing an adjustment equation that uses geometry coverage percentages of particular areas in the layout to determine an adjustment to the modification. In some embodiments, an upper layout for an upper of an IC are modified using information (such a density map) relating to a lower layout for a lower layer of the IC.

IPC 8 full level

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